Zynq-7000 All Programmable SoC

Technical Reference Manual

UG585 (v1.8.1) September 19, 2014

XILINX®

B.22 I2C Controller (IIC)

Module Name	I2C Controller (IIC)
Software Name	XIICPS
Base Address	0xE0004000 i2c0 0xE0005000 i2c1
Description	Inter Integrated Circuit (I2C)
Vendor Info	Cadence IIC

Register Summary

Register Name	Address	Width	Type	Reset Value	Description
Control_reg0	0x00000000	16	mixed	0x00000000	Control Register
Status_reg0	0x00000004	16	ro	0x00000000	Status register
I2C_address_reg0	0x00000008	16	mixed	0x00000000	IIC Address register
I2C_data_reg0	0x0000000C	16	mixed	0x00000000	IIC data register
Interrupt_status_reg0	0x00000010	16	mixed	0x00000000	IIC interrupt status register
Transfer_size_reg0	0x00000014	8	rw	0x00000000	Transfer Size Register
Slave_mon_pause_reg0	0x00000018	8	mixed	0x00000000	Slave Monitor Pause Register
Time_out_reg0	0x0000001C	8	rw	0x0000001F	Time out register
Intrpt_mask_reg0	0x00000020	16	ro	0x000002FF	Interrupt mask register
Intrpt_enable_reg0	0x00000024	16	mixed	0x00000000	Interrupt Enable Register
Intrpt_disable_reg0	0x00000028	16	mixed	0x00000000	Interrupt Disable Register

Register (IIC) Control_reg0

Name	Control_reg0
Software Name	CR
Relative Address	0x00000000
Absolute Address	i2c0: 0xE0004000 i2c1: 0xE0005000
Width	16 bits
Access Type	mixed
Reset Value	0x00000000
Description	Control Register

Register Control_reg0 Details

Field Name	Bits	Type	Reset Value	Description
divisor_a (DIV_A)	15:14	rw	0x0	Divisor for stage A clock divider. 0 - 3: Divides the input pclk frequency by divisor_a + 1.
divisor_b (DIV_B)	13:8	rw	0x0	Divisor for stage B clock divider. 0 - 63 : Divides the output frequency from divisor_a by divisor_b + 1.
reserved	7	ro	0x0	Reserved, read as zero, ignored on write.
CLR_FIFO	6	rw	0x0	1 - initializes the FIFO to all zeros and clears the transfer size register. Automatically gets cleared on the next APB clock after being set.
SLVMON	5	rw	0x0	Slave monitor mode 1 - monitor mode. 0 - normal operation.
HOLD	4	rw	0x0	hold_bus 1 - when no more data is available for transmit or no more data can be received, hold the sclk line low until serviced by the host. 0 - allow the transfer to terminate as soon as all the data has been transmitted or received.
ACK_EN (ACKEN)	3	rw	0x0	This bit needs to be set to 1 1 - acknowledge enabled, ACK transmitted 0 - acknowledge disabled, NACK transmitted.
NEA	2	rw	0x0	Addressing mode: This bit is used in master mode only. 1 - normal (7-bit) address 0 - reserved
MS	1	rw	0x0	Overall interface mode: 1 - master 0 - slave
RW (RD_WR)	0	rw	0x0	Direction of transfer: This bit is used in master mode only. 1 - master receiver 0 - master transmitter.

Register (IIC) Status_reg0

Name	Status_reg0
Software Name	SR

Relative Address	0x00000004
Absolute Address	i2c0: 0xE0004004 i2c1: 0xE0005004
Width	16 bits
Access Type	ro
Reset Value	0x00000000
Description	Status register

Register Status_reg0 Details

Field Name	Bits	Type	Reset Value	Description
reserved	15:9	ro	0x0	Reserved, read as zero, ignored on write.
BA	8	ro	0x0	Bus Active 1 - ongoing transfer on the I2C bus.
RXOVF	7	ro	0x0	Receiver Overflow 1 - This bit is set whenever FIFO is full and a new byte is received. The new byte is not acknowledged and contents of the FIFO remains unchanged.
TXDV	6	ro	0x0	Transmit Data Valid - SW should not use this to determine data completion, it is the RAW value on the interface. Please use COMP in the ISR. 1 - still a byte of data to be transmitted by the interface.
RXDV	5	ro	0x0	Receiver Data Valid 1 -valid, new data to be read from the interface.
reserved	4	ro	0x0	Reserved, read as zero, ignored on write.
RXRW	3	ro	0x0	RX read_write 1 - mode of the transmission received from a master.
reserved	2:0	ro	0x0	Reserved, read as zero, ignored on write.

Register (IIC) I2C_address_reg0

Name	I2C_address_reg0
Software Name	ADDR
Relative Address	0x00000008
Absolute Address	i2c0: 0xE0004008 i2c1: 0xE0005008
Width	16 bits

Access Type	mixed
Reset Value	0x00000000
Description	IIC Address register

Register I2C_address_reg0 Details

Field Name	Bits	Type	Reset Value	Description
reserved	15:10	ro	0x0	Reserved, read as zero, ignored on write.
ADD (MASK)	9:0	rw	0x0	Address 0 - 1024: Normal addressing mode uses add[6:0]. Extended addressing mode uses add[9:0].

Register (IIC) I2C_data_reg0

Name	I2C_data_reg0
Software Name	DATA
Relative Address	0x0000000C
Absolute Address	i2c0: 0xE000400C i2c1: 0xE000500C
Width	16 bits
Access Type	mixed
Reset Value	0x00000000
Description	IIC data register

Register I2C_data_reg0 Details

Field Name	Bits	Type	Reset Value	Description
reserved	15:8	ro	0x0	
DATA (MASK)	7:0	rw	0x0	data 0 -255: When written to, the data register sets data to transmit. When read from, the data register reads the last received byte of data.

Register (IIC) Interrupt_status_reg0

Name	Interrupt_status_reg0
Software Name	ISR
Relative Address	0x00000010
Absolute Address	i2c0: 0xE0004010 i2c1: 0xE0005010

Width	16 bits
Access Type	mixed
Reset Value	0x00000000
Description	IIC interrupt status register

Register Interrupt_status_reg0 Details

Field Name	Bits	Type	Reset Value	Description
reserved	15:10	ro	0x0	Reserved, read as zero, ignored on write.
ARB_LOST (IXR_ARB_LOST)	9	wtc	0x0	arbitration lost 1 = master loses bus ownership during a transfer due to ongoing arbitration
reserved	8	ro	0x0	Reserved, read as zero, ignored on write.
RX_UNF (IXR_RX_UNF)	7	wtc	0x0	FIFO receive underflow 1 = host attempts to read from the I2C data register more times than the value of the transfer size register plus one
TX_OVF (IXR_TX_OVR)	6	wtc	0x0	FIFO transmit overflow 1 = host attempts to write to the I2C data register more times than the FIFO depth
RX_OVF (IXR_RX_OVR)	5	wtc	0x0	Receive overflow 1 = This bit is set whenever FIFO is full and a new byte is received. The new byte is not acknowledged and contents of the FIFO remains unchanged.
SLV_RDY (IXR_SLV_RDY)	4	wtc	0x0	Monitored slave ready 1 = addressed slave returns ACK.
TO (IXR_TO)	3	wtc	0x0	Transfer time out 1 = I2C sclk line is kept low for longer time
NACK (IXR_NACK)	2	wtc	0x0	Transfer not acknowledged 1 = slave responds with a NACK or master terminates the transfer before all data is supplied
DATA (IXR_DATA)	1	wtc	0x0	More data 1 = Data being sent or received
COMP (IXR_COMP)	0	wtc	0x0	Transfer complete 1 = transfer is complete

Register (IIC) Transfer_size_reg0

Name	Transfer_size_reg0
Software Name	TRANS_SIZE
Relative Address	0x00000014
Absolute Address	i2c0: 0xE0004014 i2c1: 0xE0005014
Width	8 bits
Access Type	rw
Reset Value	0x00000000
Description	Transfer Size Register

Register Transfer_size_reg0 Details

This register's meaning varies according to the operating mode as follows:

* Master transmitter mode: number of data bytes still not transmitted minus one

* Master receiver mode: number of data bytes that are still expected to be received

* Slave transmitter mode: number of bytes remaining in the FIFO after the master terminates the transfer

* Slave receiver mode: number of valid data bytes in the FIFO

This register is cleared if CLR_FIFO bit in the control register is set.

Field Name	Bits	Type	Reset Value	Description
Transfer_Size (MASK)	7:0	rw	0x0	Transfer Size 0-255

Register (IIC) Slave_mon_pause_reg0

Name	Slave_mon_pause_reg0
Software Name	SLV_PAUSE
Relative Address	0x00000018
Absolute Address	i2c0: 0xE0004018 i2c1: 0xE0005018
Width	8 bits
Access Type	mixed
Reset Value	0x00000000
Description	Slave Monitor Pause Register

Register Slave_mon_pause_reg0 Details

Field Name	Bits	Type	Reset Value	Description
reserved	7:4	ro	0x0	Reserved, read as zero, ignored on write.
Pause (MASK)	3:0	rw	0x0	pause interval 0 - 7: pause interval

Register (IIC) Time_out_reg0

Name	Time_out_reg0
Software Name	TIME_OUT
Relative Address	0x0000001C
Absolute Address	i2c0: 0xE000401C i2c1: 0xE000501C
Width	8 bits
Access Type	rw
Reset Value	0x0000001F
Description	Time out register

Register Time_out_reg0 Details

Field Name	Bits	Type	Reset Value	Description
TO (MASK)	7:0	rw	0x1F	Time Out 127 - 32 : value of time out register

Register (IIC) Intrpt_mask_reg0

Name	Intrpt_mask_reg0
Software Name	IMR
Relative Address	0x00000020
Absolute Address	i2c0: 0xE0004020 i2c1: 0xE0005020
Width	16 bits
Access Type	ro
Reset Value	0x000002FF
Description	Interrupt mask register

Register Intrpt_mask_reg0 Details

Each bit in this register corresponds to a bit in the interrupt status register. If bit i in the interrupt mask register is set, the corresponding bit in the interrupt status register is ignored. Otherwise, an interrupt is generated whenever bit i in the interrupt status register is set.

Bits in this register are set through a write to the interrupt disable register and are cleared through a write to the interrupt enable register.

All mask bits are set and all interrupts are disabled after reset.

Interrupt mask register has the same format as the interrupt status register.

Field Name	Bits	Type	Reset Value	Description
reserved	15:10	ro	0x0	Reserved, read as zero, ignored on write.
ARB_LOST (IXR_ARB_LOST)	9	ro	0x1	arbitration lost 1 = Mask this interrupt 0 = unmask this interrupt
reserved	8	ro	0x0	Reserved, read as zero, ignored on write.
RX_UNF (IXR_RX_UNF)	7	ro	0x1	FIFO receive underflow 1 = Mask this interrupt 0 = unmask this interrupt
TX_OVF (IXR_TX_OVR)	6	ro	0x1	FIFO transmit overflow 1 = Mask this interrupt 0 = unmask this interrupt
RX_OVF (IXR_RX_OVR)	5	ro	0x1	Receive overflow 1 = Mask this interrupt 0 = unmask this interrupt
SLV_RDY (IXR_SLV_RDY)	4	ro	0x1	Monitored slave ready 1 = Mask this interrupt 0 = unmask this interrupt
TO (IXR_TO)	3	ro	0x1	Transfer time out 1 = Mask this interrupt 0 = unmask this interrupt
NACK (IXR_NACK)	2	ro	0x1	Transfer not acknowledged 1 = Mask this interrupt 0 = unmask this interrupt
DATA (IXR_DATA)	1	ro	0x1	More data 1 = Mask this interrupt 0 = unmask this interrupt
COMP (IXR_COMP)	0	ro	0x1	Transfer complete 1 = Mask this interrupt 0 = unmask this interrupt

Register (IIC) Intrpt_enable_reg0

Name	Intrpt_enable_reg0
Software Name	IER
Relative Address	0x00000024
Absolute Address	i2c0: 0xE0004024 i2c1: 0xE0005024
Width	16 bits
Access Type	mixed
Reset Value	0x00000000
Description	Interrupt Enable Register

Register Intrpt_enable_reg0 Details

This register has the same format as the interrupt status register.

Setting a bit in the interrupt enable register clears the corresponding mask bit in the interrupt mask register, effectively enabling corresponding interrupt to be generated.

Field Name	Bits	Type	Reset Value	Description
reserved	15:10	ro	0x0	Reserved, read as zero, ignored on write.
ARB_LOST (IXR_ARB_LOST)	9	wo	0x0	arbitration lost 1 = enable this interrupt
reserved	8	ro	0x0	Reserved, read as zero, ignored on write.
RX_UNF (IXR_RX_UNF)	7	wo	0x0	FIFO receive underflow 1 = enable this interrupt
TX_OVF (IXR_TX_OVR)	6	wo	0x0	FIFO transmit overflow 1 = enable this interrupt
RX_OVF (IXR_RX_OVR)	5	wo	0x0	Receive overflow 1 = enable this interrupt
SLV_RDY (IXR_SLV_RDY)	4	wo	0x0	Monitored slave ready 1 = enable this interrupt
TO (IXR_TO)	3	wo	0x0	Transfer time out 1 = enable this interrupt
NACK (IXR_NACK)	2	wo	0x0	Transfer not acknowledged 1 = enable this interrupt
DATA (IXR_DATA)	1	wo	0x0	More data 1 = enable this interrupt
COMP (IXR_COMP)	0	wo	0x0	Transfer complete Will be set when transfer is complete 1 = enable this interrupt

Register (IIC) Intrpt_disable_reg0

Name	Intrpt_disable_reg0
Software Name	IDR
Relative Address	0x00000028
Absolute Address	i2c0: 0xE0004028 i2c1: 0xE0005028
Width	16 bits
Access Type	mixed
Reset Value	0x00000000
Description	Interrupt Disable Register

Register Intrpt_disable_reg0 Details

This register has the same format as the interrupt status register.

Setting a bit in the interrupt disable register sets the corresponding mask bit in the interrupt mask register, effectively disabling corresponding interrupt to be generated.

Field Name	Bits	Type	Reset Value	Description
reserved	15:10	ro	0x0	Reserved, read as zero, ignored on write.
ARB_LOST (IXR_ARB_LOST)	9	wo	0x0	arbitration lost 1 = disable this interrupt
reserved	8	ro	0x0	Reserved, read as zero, ignored on write.
RX_UNF (IXR_RX_UNF)	7	wo	0x0	FIFO receive underflow 1 = disable this interrupt
TX_OVF (IXR_TX_OVR)	6	wo	0x0	FIFO transmit overflow 1 = disable this interrupt
RX_OVF (IXR_RX_OVR)	5	wo	0x0	Receive overflow 1 = disable this interrupt
SLV_RDY (IXR_SLV_RDY)	4	wo	0x0	Monitored slave ready 1 = disable this interrupt
TO (IXR_TO)	3	wo	0x0	Transfer time out 1 = disable this interrupt
NACK (IXR_NACK)	2	wo	0x0	Transfer not acknowledged 1 = disable this interrupt

Field Name	Bits	Type	Reset Value	Description
DATA (IXR_DATA)	1	wo	0x0	Master Write or Slave Transmitter Master Read or Slave Receiver 1 = disable this interrupt
COMP (IXR_COMP)	0	wo	0x0	Transfer complete Will be set when transfer is complete 1 = disable this interrupt